DELAMINATION OF PB-FREE FLIP CHIP UNDERFILL DURING 2ND LEVEL INTERCONNECT REFLOW

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ABSTRACT

In this paper, the delamination of Pb-free flip chip underfill during the 2nd level interconnect reflow is investigated experimentally. To acquire the adhesion characteristics of underfill at high temperature, the interfacial fracture toughness is calculated through experimental and numerical works. The CMM (Compact Mixed Mode) specimen with an initial crack between chip and underfill is used to measure the critical force at Mode-I, II and mixed-mode loading conditions. Since the 2nd level solder reflow occurs around 250 $^{\circ}C$, the fracture tests are performed according to temperature increase. The critical forces obtained from tests are used as loading condition in finite element analysis, and the fracture toughness such as the critical strain energy release rate and the critical stress intensity factor are calculated by the modified crack closure integral. Finally, the interfacial fracture toughness at high temperature is compared with that by finite element analysis of Pb-free solder phase change in order to examine whether the crack will initiate or propagate by volume expansion due to phase change of Pb-free solder or not.

INTRODUCTION

Nowadays, the interfaces are numerous in flip-chip packages (i.e. die/passivation, passivation/underfill, underfill/solder mask, and solder mask/substrate) and susceptible to delamination which is driven by residual thermal stress during cooling from processing temperatures and from thermal cycling during device operation [1]. Therefore, the proper characterization of interfacial adhesion strength is very important for reliability prediction as well as process control in the flip-chip electronic packages [2,3]. The efforts to calculate fracture toughness at the interfaces, especially bimaterial interfaces, have been done by using various specimen types, e.g. SCB (single cantilever beam) [2], SENB (single-edge notch bend or three-point bending) [3], UENF (unsymmetric end-notched flexure) [4], DCB (double cantilever beam) [5], CMM (Compact Mixed Mode) [6], Brazil-nut [7] etc. Chen et al. employed a composite beam on an elastic foundation to determine critical strain energy release rate [2]. Kuhl et al. presented an experimental technique using sandwiched Brazil-nut specimens to obtain the interfacial fracture toughness as a function of loading phase angle [7]. And some analytical methods such as plate theory [4] and corrected beam theory with consideration of transverse deformation and crack tip singularity [8] were utilized with finite element analysis to calculate interfacial fracture toughness. Sun et al. compared stress intensity factors for bimaterial panel with a center crack based on both oscillatory and contact models [9]. Dauskardt et al. measured the adhesion and interfacial fracture resistance of SiO_2/TiN interfaces in thin film structures [1].

Considering the methods to calculate fracture toughness from finite element analysis, the following methods can be referred. As an energy method, CCI(crack closure integral) [9], MCCI(modified crack closure integral) [10] and MVCEM(modified virtual crack extension method) [11] are representative, and CSDRM(crack surface displacement ratio method) [9], MCSDEM(modified crack surface displacement extrapolation method) [12] are also used for evaluating interfacial fracture toughness. From the literature survey, it can be known that the critical strain energy release rate (G_c) between chip and underfill is about 30 J/m^2 [2], 35 J/m^2 [3] and 4~68 J/m^2 [13] which is dependent on the materials of Si passivation and underfill, and the interfacial bond strength is in the range of 7~25 MPa [14].

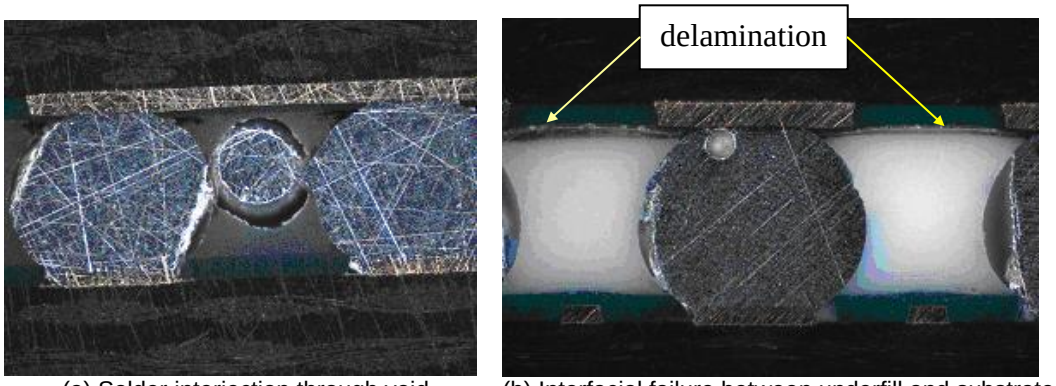
In this paper, the probability of delamination at the interfaces chip/underfill or substrate/underfill during the 2nd interconnect solder reflow process is studied. When Pb-free solders are used in both 1st and 2nd level interconnects in sequential stages, the solder bump in flip chip solder interconnect may melt during the 2nd level interconnect because most of Pb-free solders have similar melting temperature range of 220~240 $^{\circ}C$. Due to the phase change of Pb-free solder bump from solid to liquid,

high hydrostatic pressure is applied on the surrounding materials, and the bridging of the adjacent flip chip solders by the interjected solder through the delamination is issued as a new reliability concern. The authors analyzed two kinds of crack models, i.e. interfacial crack and through-the-crack models to quantify the effect of the volumetric expansion of Pb-free solder, and also showed the interjection of molten solder and the interfacial failure of underfill after thermal cycling experiment [15]. However, the interfacial fracture toughness around solder reflow temperature is not available yet, so the authors aim to measure the interfacial fracture toughness at high temperature to compare it with the corresponding fracture parameter resulted from finite element analysis. Celemin et al. explained that the decrease of fracture strength and toughness of a 2-D woven Nicalon/Al_2O_3 matrix composite from ambient to 800 $^{\circ}C$ was caused by the localized interface oxidation and the degradation of the fiber strength [16]. Ikeda et al. showed that the delamination toughness decreases remarkably with the increase of temperature for the interface between ACF(anisotropic conductive film) and Al-pattern/substrate [11].

EXPERIMENTS

Underfill delamination

Pb-free FC-PBGA samples are prepared to observe the delamination or crack around solder after its phase change. To visualize a failure more clearly, BGA SAC(Sn-Ag-Cu) solder balls between substrate and PCB are underfilled instead of the small scale flip chip solder bumps. The package goes through a typical reflow cycle with the peak temperature 250 $^{\circ}C$, and then it is cooled down to room temperature. To see the delamination and the void shape, the cross-section of FC-PBGA is exposed as shown in Fig.1. It can be seen that a part of solder moved to the adjacent void as shown in Fig.1(a) and the interfacial failure between substrate and underfill occurred as shown in Fig.1(b). Therefore, these results show that the reflow of Pb-free solder can raise a serious reliability issue due to the generation of delamination and solder bridging.



(a) Solder interjection through void (b) Interfacial failure between underfill and substrate

Figure 1. Cross-section pictures around solder balls of FC-PBGA

Fracture toughness testing

In this section, the relation between temperature and interfacial fracture toughness ($G_c, K_{Ic}(K_{IIc})$) is examined by using Si/UF/Si CMM specimen and loading fixture shown in Fig.2. High temperature measurement is performed in the environmental chamber whose maximum running temperature is 300 $^{\circ}C$. A 4 inch diameter Si wafer with 5 μm thickness polyamide passivation layer is washed using alcohol, DI water, and then dried by Nitrogen gas. The thermal tape is stuck on the bottom wafer to control the thickness of underfill material layer. 4 mil thickness of underfill layer is designed because the solder bump is typically 75-100 μm high for flip chip packaging. In predetermined areas, the thermal tape is used as mask, and Frekote release agent is laid on the specific area at room temperature with clean lint-free paper in order to create a pre-existing crack. After the release agent is cured, the thermal tapes as mask are tore from the Si wafer and underfill material is applied by syringe. The enough pressure, which helps reduce the possibility of bubble in underfill layer, is required in covering top Si wafer on the underfill material. The T_g of this underfill material is about 150 $^{\circ}C$, and it is cured at 165 $^{\circ}C$ for an hour. The Si/UF/Si sandwich sample is diced into requested test vehicle dimension one inch long and a quarter inch wide. A half inch pre-existing crack is used, and the sample is baked in the oven for two hours in order to remove the moisture. The image from C-SAM (Scanning Acoustic Microscope) shown in Fig.3 is taken to examine for any voids in the underfill layer. Two-part epoxy is used to stick a test vehicle on two steel blocks and two steel blocks are connected to the fixture by bolt and nut. In other words, the load is applied on the test vehicle through the fixture and steel blocks. The procedure for sample preparation is shown in Fig.4.

Figure 2. Bi-material CMM specimen and fixture

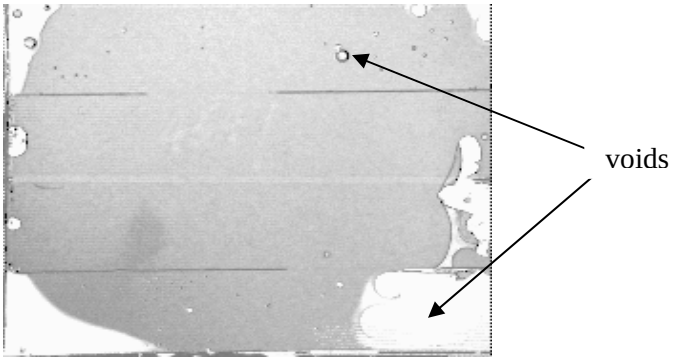


Figure 3. CSAM image used to check voids inside sample

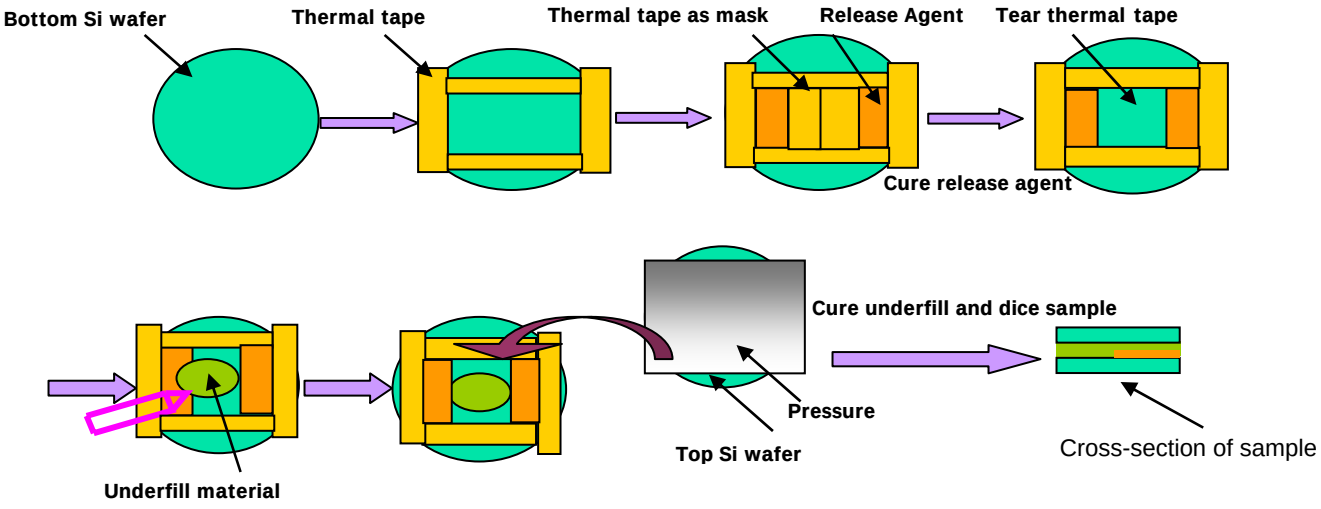


Figure 4. Procedure for sample preparation

According to the fixture, the load can be applied at 0°, 22.5°, 45°, 67.5° and 90° using MTS machine. And the experiments are performed at room temperature, 100 $^{\circ}C$, 150 $^{\circ}C$, 200 $^{\circ}C$, and 250 $^{\circ}C$. The displacement rate 1 mm/min is used as loading condition. In this experiment, the effects of moisture and displacement rate change are not considered. In each different loading angle and thermal condition, three test vehicles are used and the average load is considered as the critical force. Currently, the authors are finding another epoxy with stronger adhesion strength at high temperature because a delamination at the interface between chip and steel block precedes crack propagation at the pre-existing crack surface. So, some critical forces measured at 25 $^{\circ}C$, 100 $^{\circ}C$ and 150 $^{\circ}C$ are presented in Table 1 for mode-I loading condition. It can be seen that the critical force is reduced as temperature increases. The critical force is applied in finite element model to calculate the critical strain energy release rate.

Table 1. Critical force and strain energy release rate for mode-I

Temperature ($^{\circ}C$)	Critical force (N)	G_c (J/m^2)
25	370	2.53
100	351.5	2.28
150	256.4	1.22

NUMERICAL MODELING AND RESULTS

Phase change of Pb-free solder

In this section, the problem considered in our previous work [15] and the numerical modeling and results to be compared with experimental data are described. Figure 5 shows the finite element model with a pre-existing interfacial crack where only one solder is considered by assuming an axisymmetric condition. The dimensions of a solder ball are 4 mil diameter at top/bottom pad sides and 5.5 mil diameter at the bulge, and 0.5 mil initial crack is assumed as shown in Fig.5. Linear fluid elements and quadratic solid elements are used for modeling the solder and the other materials surrounding solder, respectively. The contact constraint condition is assigned at the interface between solder and neighboring materials and the crack surfaces. The material properties of each material are shown in Table 2. The CTE of solder is calculated considering effective volume expansion in the amount of 4.1% during phase change.

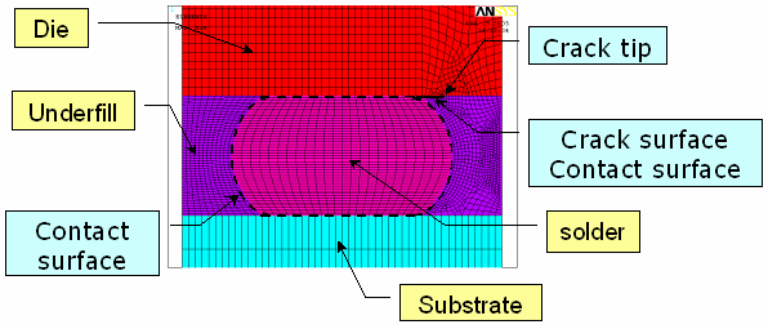


Figure 5. Finite element mesh of interfacial crack model

Table 2. Mechanical properties of materials used

	Young's modulus ($\times 10^6$ psi)	Poisson's ratio	CTE (ppm/℃)
Silicon die	23.5	0.28	3
Ceramic substrate	43.5	0.23	8
Organic substrate	3.77	0.39	15
Underfill Hysol FP4527	7.252×10^{-3} (above T_g) 7.964×10^{-1} (below T_g)	0.33	88 (above T_g) 26 (below T_g)

Solder (pure tin)	4.14 (Bulk modulus)	-	4556 (232~235 $^{\circ}C$)

Fig.6 shows that normal stress σ_{xx} is concentrated at the crack tip. Strain energy release rates for mode-I and mode-II are $G_I = 0.08(J/m^2)$ and $G_{II} = 0.22(J/m^2)$, respectively. Accordingly, the total strain energy release rate is $G_T = 0.3(J/m^2)$ and it can be seen that in-plane shear is more dominant than in-plane tension in this analysis.

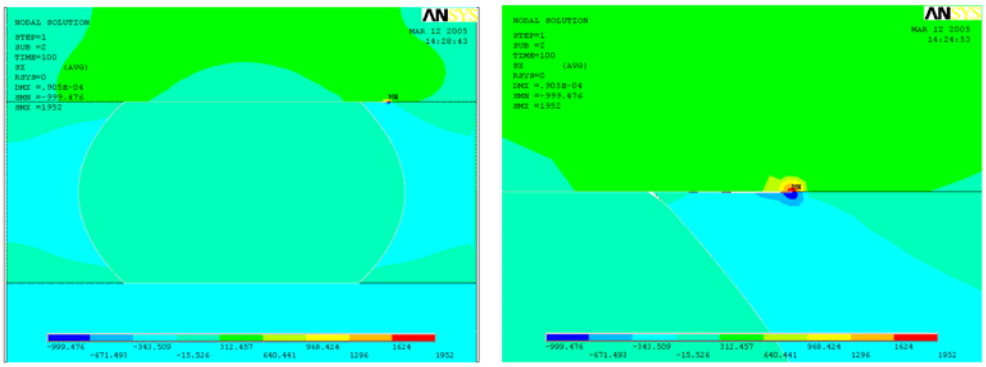


Figure 6. Stress σ_{xx} distribution (right figure is the enlarged one)

Interfacial fracture toughness

The finite element model consists of chip, underfill and steel blocks, and the deformed meshes in mode-I loading condition are shown in Fig.7. Plane strain condition is assumed and constant pressure that is equivalent to critical force is applied at top and bottom surfaces. The element size near crack tip is about 1% of crack length. The normal stress σ_{yy} distribution at room temperature is displayed in Fig.8. The strain energy release rate is calculated by modified crack closure integral and those values at 25 $^{\circ}C$, 100 $^{\circ}C$ and 150 $^{\circ}C$ are presented in Table 1. As is expected, the critical strain energy release rate is reduced according to temperature increase. To compare G_c with $G_T = 0.3(J/m^2)$ from phase change simulation of Pb-free solder, the critical strain energy release rate at 250 $^{\circ}C$ is supposed to be calculated.

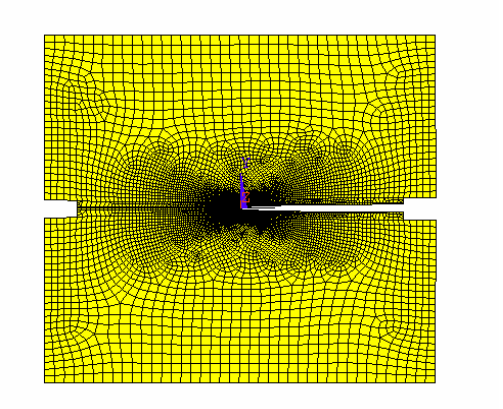


Figure 7. Deformed finite element meshes in mode-I condition

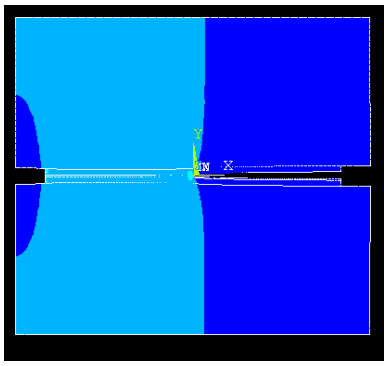


Figure 8. Stress σ_{yy} distribution

CONCLUSIONS

In this paper, the interfacial fracture toughness such as the critical strain energy release rate is calculated at high temperature by using CMM fracture toughness testing and finite element analysis. An initial crack between chip passivation layer and

underfill is created. The fracture testing is performed at various loading angles and temperature conditions to acquire the critical forces. The interfacial fracture toughness is calculated by modified crack closure integral and is compared with the strain energy release rate at an interfacial crack due to phase change of Pb-free solder during 2nd level interconnect reflow. It can be confirmed in mode-I loading condition that G_c is reduced as temperature increases. It will be seen whether the phase change of Pb-free solder will cause delamination between chip and underfill or not after G_c at solder reflow temperature is obtained. Since Young's modulus affects the calculation of strain energy release rate, the measurement of Young's modulus of underfill at high temperature will be carried out for accurate finite element analysis.

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