

MECHANICAL FAILURE IN MICROELECTRONIC PACKAGING

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SUMMARY: in this paper an overview of microelectronic devices, namely the so-called electronic packagings, their mechanical failure mechanisms, possible fracture mechanics-based design approaches and experimental characterization is given with the aim to get insight of a subject that nowadays shows an increasing interest from the international scientific community.

INTRODUCTION

It is a matter of fact that in the last few years the use electronic-based devices has been playing an increasingly relevant role in our day-to-day life. Besides, in order to hinder the strong competition in this market, the performance requirements have been following the same trend. Such conditions impose reduced time-to-market and engineering costs for new products, that means a shorter time for validation of new solutions and reliability assessment. For this reason, failure of microelectronic devices has become in this last decade a prominent field of research all over the world. A “physics of failure” approach based on a scientific determination of the dominant failure mechanisms and failure sites within the component is generally accepted. The results of this physics of failure analysis allow a designer to choose package geometries and materials which reduce the risk of failure by the identified mechanisms. This makes reliability assessment a part of the design process rather than just a tool for predicting the useful life of an existing product.

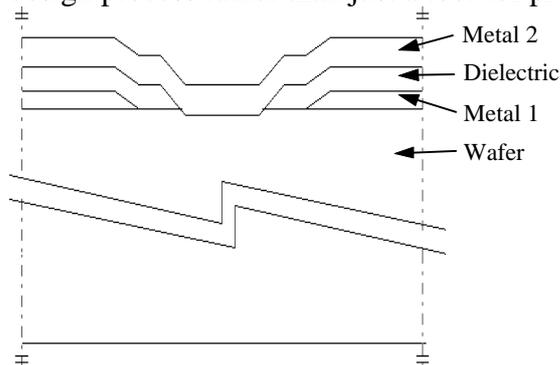


Fig. 1: example of chip cell section connections. (the width is of the order of 50 μm).

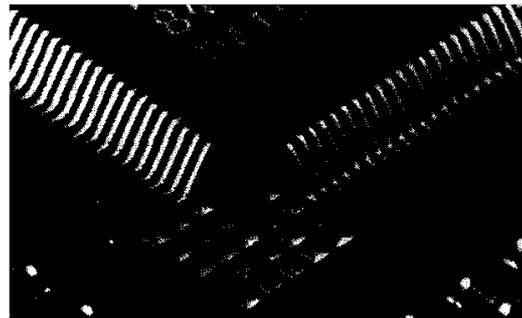


Fig. 2: example of wirebond chip connections. (Dudek et alii, 1995). Wire diameter is 0.5 mm.

A technically and economically relevant branch of electronic devices is constituted by the so-called electronic packaging, that is when the circuitry is permanently plastic encapsulated or inserted in a ceramic housing. The purpose is to protect the relatively brittle device heart (normally a single or multichip plate), against mechanical and environmental injuries and ensure electrical isolation. Packages typically include a chip

(called also die), which contains the primary circuit elements; the chip is composed by many elementary cells of the kind reported in Fig. 1. Other elements are die attach, lead frame, leads, wires, substrate, passive elements, substrate attach, wire bonds, interconnection wiring and case. The die is attached to substrate by a die attach composed usually of gold, epoxy, polyimide or solder alloy. The substrate provides the mechanical support to the die and acts as heat carrier to the package case. In the so-called hybrid packages, it may also contain printed routing paths (metal lines or metallizations) and passive components. In this case the basic components are a Si wafer where Al-Si, Al-Cu or Al-Si-Cu thin stack (on the order of 1 μm height) are deposited on to create the circuit; those stacks are normally isolated by a sputtered ceramic or glass dielectric layer less than 1 μm height. Depending on the device, the die is connected to the substrate or to the lead frame pads through Cu wires (about 0.5 mm diameter) that are soldered with a Sn-Pb alloy (Fig. 2, Dudek *et alii*, 1995) or by a leaded tape to allow for an easier automated mounting; the processes are called wire bonding or tape automated bonding (TAB), respectively. An alternative wireless method, where the chip is connected by many small ball solder joints, is called flip-chip bonding. The whole assembly is finally sealed in a case that provides structural rigidity and avoids contaminants income.

The aim of this paper is to identify possible failure in microelectronic packagings whose assessment involves the use of fracture mechanics and review experimental techniques for the fracture characterization of specific parts in such devices.

GENERALITIES ON MICROELECTRONIC PACKAGING MECHANICAL FAILURE

Failures in microelectronic devices are often classified into electrical, mechanical, and corrosion failures. The mechanical ones normally cause the loss of device functionality well before the visible breaking of the device. The CALCE research group at the University of Maryland (USA) that operates on this subject since 1991, produced a detailed summary of possibly failure-affected parts in electronic devices and the related mechanisms, of which a scheme is given in Fig. 3. One can see that in the majority of cases the failure is clearly due to fatigue and/or fracture. Heat generated by Joule's effect during transient and steady-state conditions causes a mismatched thermal dilatation between the many different materials fit together and the repeated on-off operation originates thermomechanical fatigue and a subsequent cracking phenomenon. Furthermore, in plastic encapsulated devices initial residual stresses are induced by the packaging resin shrinkage after cooling due to assembly-resin mismatch. The same kind of problem can be found in the reflow soldering process, where hot (up to 250°C) air is used to melt the solder. Examples of fracture failures in specific packaging assemblies are given in the remainder of the section.

Plastic Encapsulated Devices (PEDs)

The use of PEDs (Fig. 4, Pendse, R.D., 1991) is widespread in the electronic industry because of their low cost and ease of manufacture. Unfortunately, the packaging operation induces stresses on the chip. The origin is due to the mismatch in thermal expansion coefficients of the various materials involved along with the fact that they are

joined in a stress-free state at temperatures other than room temperature (e.g.: die attach, 175°C; wire bonding 150°C; encapsulant resin molding, 175°C, ...).

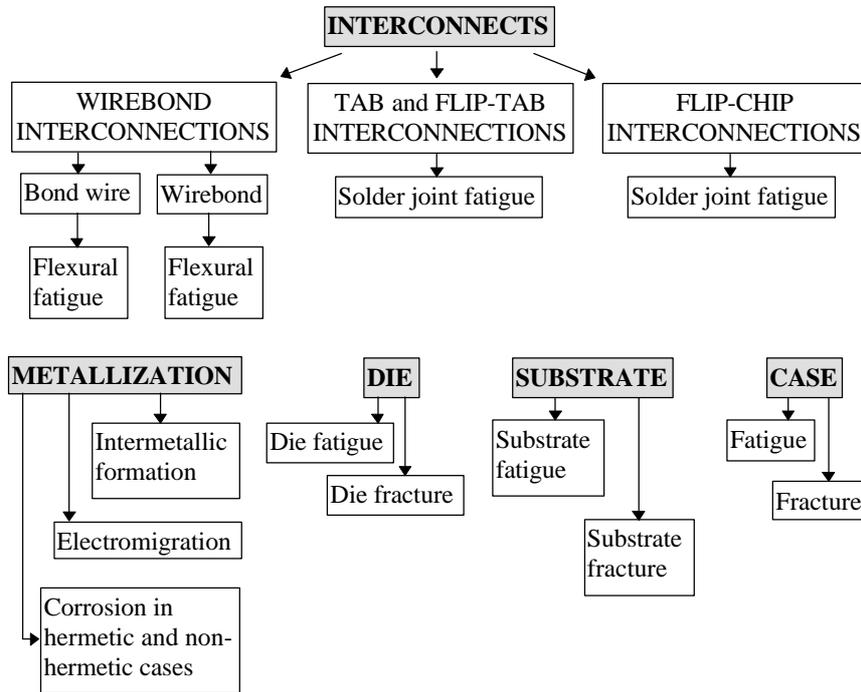


Fig. 3: summary of failure mechanisms in microelectronic packagings.

Damage develops in the interconnect features on die surface (dielectric cracking, metal lines deformation, ...) usually resulting in shorts or current leakage between metal layers. The damage by surface shear and is normally more critical for the largest chip sizes, being the wide the chip the high the stress at corners. Pendse (Pendse, 1991) attempted to assess this problem by executing an interconnect damage test, where a two metal layers chip resembling the architecture of interest (in the specific case, CMOS, see also Fig. 1) was fabricated with a variety of bond pads at corners to simulate different structures of interest and tested with a uniform temperature cycling. Failure occurs typically when the intermediate dielectric cracks, thus allowing for leakage currents. These latter were measured by applying a voltage bias across bond pads of structure of interest.

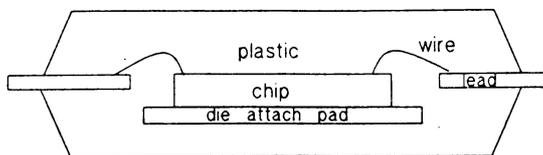


Fig. 4: scheme of a plastic encapsulated device (Pendse, R.D., 1991).

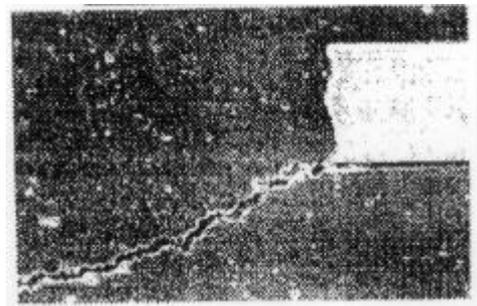


Fig 5: example of cracking in a PED (Hong et alii, 1995).

The comparison of an acceptable failure rate with the stress in the corresponding structure obtained by FEA allows to establish a semi-empirical failure criterion in term of

peak shear stress at corners. From the package viewpoint, failure appears as interfacial delamination and/or bulk cracking: delamination starts normally from an initial adhesion defect or a blister due to moisture release; cracking often occurs at sharp edges (see Fig. 5, Hong *et alii*, 1995) after thermal cycling. Amagai (Amagai, 1996) found that the same kind of failure may occur inside the IC, that is the smallest dimensional level in the device (layer heights range from 10 to less than 1 μm), with cracks starting at sharp corners in the chip layers. Treatment of such problems requires the study of stress concentration at singularity points (interfaces and corners between dissimilar materials) and the use of fracture mechanics.

LOC (lead-on-chip) packages

A typical example of cracking in a multi-layer structure device is given by LOC (lead-on-chip) package. In this technology the lead frame fingers are attached to the surface of an on-chip deposited polyimide layer by mean of a double-sided adhesive tape. The polyimide film has a stress buffering and adhesion enhancer function and furthermore protects the chip and circuits from package-induced stresses and corrosion failure. The dominant failure is the fracture in the passivation layers and metal lines following the polyimide cracking, (Fig. 6, Amagai, 1995). After a high temperature mounting process, the adhesive tape shrinks during the cooling down to room temperature; the stresses originated by the mismatched shrinking cause tape-resin delamination and damage severely the polyimide stack. This damage turns quickly into crack propagation because of the working thermal cycling. In this case, the reliability assessment can make use of fracture mechanics.

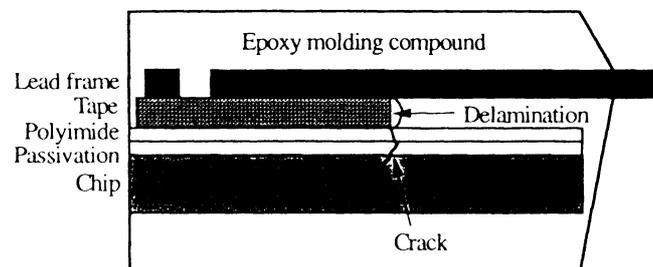


Fig. 6: section of LOC package and typical failure mode (Amagai, 1995).

Multichip modules

The density and speed required by the modern devices often lead to multichip module architectures. Such architectures concentrate in a unique device a large number of chips, with a consequent high dissipated power per unit volume. An example of multichip module is the IGBT (integrated gate bipolar transistor) device, where every single chip (2-3 cm^2) is constituted by a few hundred thousands MOS cells. In (De Lambilly, Keser, 1993) an IGBT (Fig. 7, De Lambilly, Keser, 1993) is subjected to power cycling and temperature on the chip and voltage drop across the device (V_{ce}) are used as failure indicators. A slight increase in chip temperature and V_{ce} indicates cracks growing in solder layers. Results of experiments showed that the thermal mismatch between coating and the underlying assembly causes chip wirebonds shearing up to rupture. Moreover, the bending of the whole assembly due to a bimetallic effect between the thick copper base and the other layers causes cracks to develop at copper bridges in the copper bonded layer.

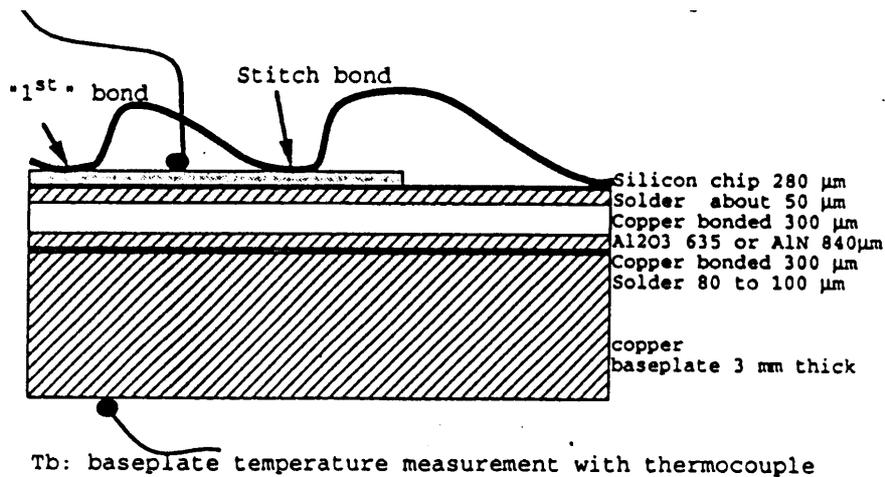


Fig. 7: scheme of an IGBT module and temperature measurement setup (De Lambilly, Keser, 1993).

FRACTURE MECHANICS DESIGN APPROACH

The use of specific guidelines for device design from the mechanical stand-point may avoid the introduction of unsatisfactory configurations leading to unexpected damage and failure occurrence. A short overview of fracture mechanics applications to the assessment of specific parts of the package is given in this section.

Die Fracture

The die, the substrate or the leadframe and the case of a microelectronic package, typically have different thermal expansion coefficients. For example, die are usually made of silicon, gallium arsenide, or indium phosphide, while the substrate is typically alumina, berylia, or copper. As the temperature cycle magnitude rises during temperature and power cycling, tensile stresses are developed in the central portion of the die and shear stresses are developed at the edges of the die. A preexisting defect may develop into a crack under the influence of thermal cycling in the die, leading to ultimate fracture of the brittle die when surface cracks at the center of the die or at the edge of the die reach their critical size. Vertical cracking of the die is caused by tensile stresses and horizontal cracking is caused by high shear stresses at the edges. Microcracks are often inserted in the die during manufacture. The thermomechanical stress level in the die has been investigated by various authors, like (Bolger, 1984), who tried to estimate with simple equations the stress acting on the die due to the substrate-die bimetallic effect. The stress level can then be used to calculate the stress intensity factor and the number of cycles to failure for a cyclic propagating crack is typically estimated with by Paris's power law:

$$\frac{da}{dN} = A(\Delta K)^n \quad (1)$$

where A and n are material properties.

Die attach cracking

The formation of randomly distributed voids at the die substrate interface is generally unavoidable during the die attach process. These voids can act as microcracks, which propagate during power cycling resulting in debonding of the die from the substrate or the substrate from the case. In other instances, vertical die attach cracking follows from stresses induced by shrinkage after the high temperature attachment process. This damage may turn quickly into crack propagation because of the working thermal cycling with a consequent fracture of the underlying the passivation layers and metal lines. A model of crack growth has been proposed by (Amagai, 1995), for the case of LOC package: a global (opening + shearing mode) SIF has been determined at the tape-polyimide-resin junction point using a FE model in which an initial delamination between resin and tape was modeled. The proposed crack growth model based on the formula:

$$\left(\sigma_{\text{eq}} r_d\right)^A N^B = t U_R \quad (2)$$

where σ_{eq} is Von Mises equivalent stress, t the layer thickness, U_R the specific mechanical energy to break the material and the radius of a damaged zone around the crack tip according to the equation:

$$r_d = \frac{1}{2\pi} \left(\frac{\Delta K}{\sigma_y} \right)^2 \quad (3)$$

Cracking in plastic packages

Thermal coefficient of expansion (CTE) mismatches drive the failure mechanisms of cracking of plastic packages. The shrinkage after encapsulation imposes a compressive stress on the die, and tends to load the molding compound in tension. Cracks therefore have a tendency to propagate in the molding compound since thermal cycling generates additional tensile stresses. Cracks also initiate due to voids in the molding compound. A detailed study of interfacial and corner stresses is reported in (Amagai, 1996). The stress field at the corner is characterized by a singular distribution of the kind:

$$\begin{aligned} \sigma_r^i &= K r^{(p-1)} g_{(\vartheta)}^i \\ \sigma_{\vartheta}^i &= K r^{(p-1)} f_{(\vartheta)}^i \\ \tau_{r\vartheta}^i &= K r^{(p-1)} f_{(\vartheta)}^i \left[h_{(\vartheta)}^i - f_{(\vartheta)}^i \right] \end{aligned} \quad (4)$$

where $i = 1, 2$ indicates the material and K is the stress intensity factor (SIF) defined as:

$$K = \lim_{r \rightarrow 0} \frac{\sigma_{\vartheta} \big|_{\vartheta=0}}{r^{(p-1)}} \quad (5)$$

p is the order of stress singularity (which depends on geometry and materials), f and h are functions depending on adjoining materials. Propagation can be modeled with Paris law. Delamination is the failure mechanism which occurs between the die and molding compound, and between the molding compound and the lead frame due to shrinkage

after molding. The delamination failure can be assessed through the use of fracture mechanics as well (see also the following section).

EXPERIMENTAL TECHNIQUES

In the previous sections it has been demonstrated that the problem of fracture, and namely interfacial fracture, is of great concern for the reliability of electronic packagings. As some analytical formulations have been there briefly reviewed, a short summary of experimental techniques for the fracture characterization of bimaterial interfaces is therefore presented in this section.

The problem of the interface separation due to cyclic stresses is experimentally studied (Amagai, 1995), (Amagai, 1996), (Shang, 1996) within the framework of interfacial LEFM (Linear Elastic Fracture Mechanics), which provides (mathematically) complex singular solution of stress fields at the crack tip as a function of jointed materials and applied stress conditions. The SIF is a complex quantity given by:

$$K = Y\sigma\sqrt{a}\left(a^{-i\varepsilon}\right) \quad (6)$$

where ε is a property depending on the adjoining materials and is zero for an homogenous material. Mode I and II SIFs depend upon K as (r = distance from the crack tip along the crack plane):

$$Kr^{i\varepsilon} = K_I + iK_{II} \quad (7)$$

and the local phase angle at the crack tip is:

$$\phi = \tan^{-1}\left(\frac{K_{II}}{K_I}\right) = \varepsilon \ln\left(\frac{r}{a}\right) \quad (8)$$

This implies the even under remote mode I loading a mixed opening + shearing mode is present at the crack tip.

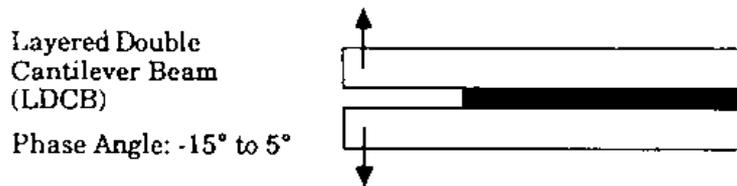


Fig. 8: LCDB specimen outline (Shang, 1996).

Interfacial isothermal FCG experiments can be conducted using LCDB (Layered Double Cantilever Beam) in (Shang, 1996), (Fig. 8, Shang, 1996). This specimen provides loading conditions very close to mode I for most materials. If the interlayer is much thinner than the outer beams, the solution for an homogeneous material can be used to calculate the strain energy release rate for the interface crack. The crack starter is normally a Chevron notch. An alternate way to the problem of starting is to introduce a flaw by placing a shim on an interface before joining. A major drawback of this specimen is possibility for the crack to assume an alternate path during propagation, i.e. changing

the from the upper to the lower interface and viceversa. This leads to a larger scattering in crack growth measurements, and overestimation of FCG threshold. A regular crack can be obtained using the flexural peel specimen (Fig. 9, Shang, 1996), which allows to achieve a wide range of crack tip loading conditions by selecting the thickness of the two beams. The detailed description of specimen preparation and FCG testing procedure has been given in (Yao, Shang, 1996). Crack growth velocity is normally expressed as a function of energy release rate range ΔG and phase angle ϕ ; the observed trend is similar to homogenous materials, that is ΔG - da/dN data can be approximated on most of the range by a power-law function of the Paris type, while there are two asymptotes for the lowest and highest values of ΔG .

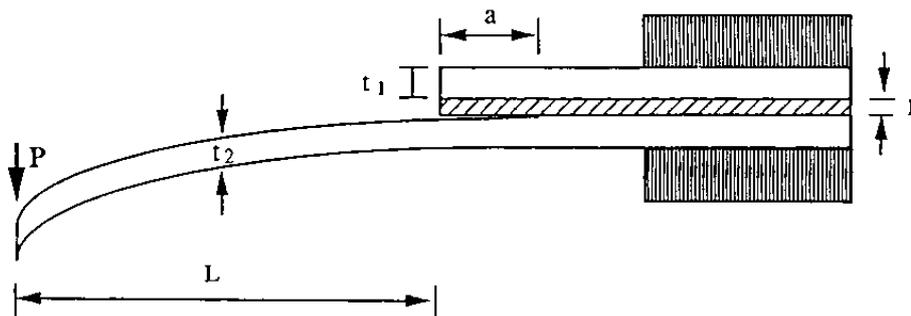


Fig 9: flexural peel specimen outline (Shang, 1996).

In (Liu *et alii*, 1995) fracture behaviour of an alumina-silver filled epoxy-glass interface was characterized with the three-point bending technique (3PB) (Fig. 10, Liu *et alii*, 1995). Details on specimen and experimental procedure are given. For that material assembly, it was found that the crack propagates either into the glass or along the glass-epoxy interface depending on the applied temperature and notch depth. In (Liu, 1995) ENF and MENF (Modified End Notched Flexural) specimens (Fig. 11) have been used to assess fracture behaviour of a copper-resin interface. Load-deflection curves were recorded to calculate the fracture toughness in term of the strain energy release rate G and to serve as a basis for a FE model response calibration.

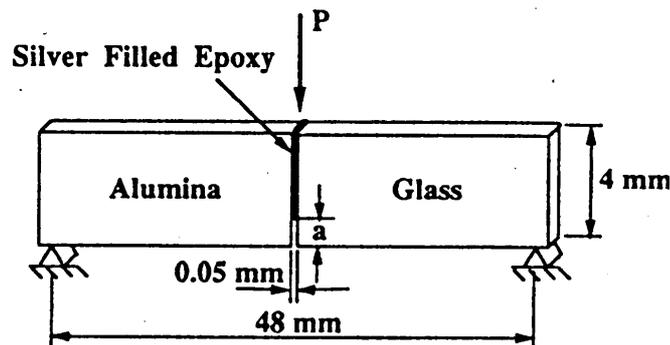


Fig. 10: layered 3PB specimen outline (Liu *et alii*, 1995).

The effect of bimaterial thickness on flow and fracture behaviour of a Sn/Pb solder alloy has been tested in (Skipor *et alii*, 1995) by mean of layered compact tension (CT)-like specimens (Fig. 12, Skipor *et alii*, 1995), of which the preparation details are given in the reference. The change from the very ductile to brittle behaviour and the increase of

resistance can be expressed as a function of the layer height and define the point after which the stress field inside the joint is no longer influenced by the interface.



Fig. 11: ENF (a) and MENF (b) specimens outline.

CONCLUSIONS

Mechanical failure mechanisms, possible fracture mechanics-based design approaches and experimental techniques for the characterization of specific parts of microelectronic packagings have been shortly reviewed. It has been shown that fracture mechanics can give a relevant contribution to the interpretation and assessment of failure even in these unusual, from the mechanical point of view, devices. The use of specific models that takes into account the typical multi-material composition of such assemblies will be the matter of researches in the near future.

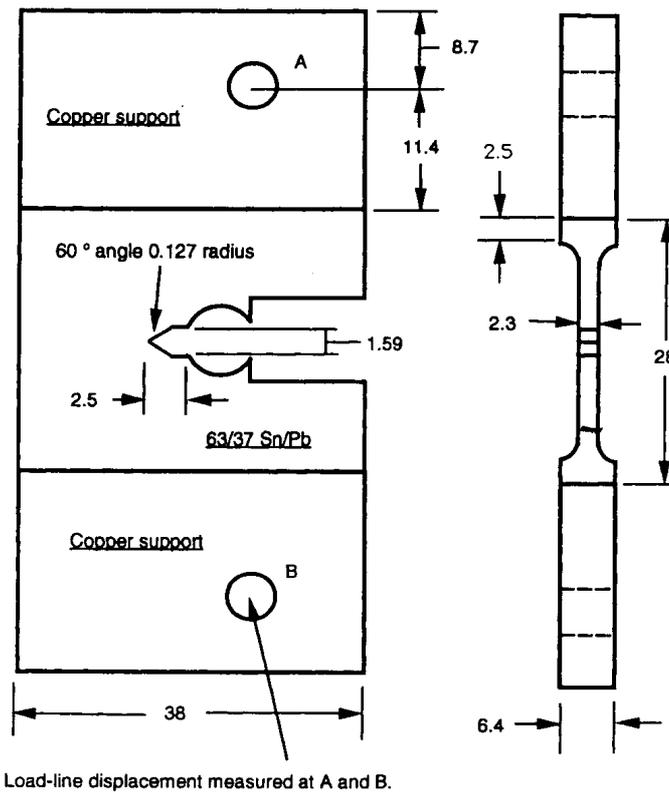


Fig. 12: CT-like specimen for testing the influence of solder alloy layer height on its flow and fracture behaviour (Skipor et alii, 1995).

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