Evaluation on the Factors Influencing Thermal-stress-induced Growth of Sn Nanowires

Yuan Li[1,*], Kentaro Miura[1], Shien Ri[2], Masumi Saka[1]

[1] Department of Nanomechanics, Tohoku University, Sendai 980-8579, Japan
[2] National Institute of Advanced Industrial Science and Technology, Tsukuba 305-8568, Japan
* Corresponding author: liyuan@ism.mech.tohoku.ac.jp

Abstract By employing a multilayer thin film structure composed of thermally oxidized Si substrate and sputtered Sn film, a series of thermal annealing experiments are carried out to challenge the synthesis of Sn nanowires following thermal-stress-induced method. The effects of two vital influencing factors, i.e., surface morphology of Sn film and annealing conditions, are explored systematically. For Sn films with either isolated islands or voids in grain boundaries, there is no any change on surface morphology after annealing. Such behavior can be attributed to the existence of gaps among islands or voids in grain boundaries, which make it difficult to generate sufficient stress to grow Sn nanowire. On the other hand, for Sn films with dense grains or coalescent islands, the occurrence of hillocks or whiskers after annealing at high temperature indicates that the proper control of surface morphology of Sn film and thermal annealing conditions may grow Sn nanowires with large aspect ratio.

Keywords Atomic migration, Influencing factors, Metallic nanowire, Thermal stress

1. Introduction

The study of Sn nanowires has been motivated by the attractive properties of bulk Sn including excellent ductility, electrical conductivity, resistance to corrosion, and its extensive application in electronics industry. Recent experimental studies [1-6] have shown that Sn nanowires have unique superconductivity and magnetic properties, which indicates their potential application in superconductors. Moreover, vertical arrays of Sn nanowires have been expected to be ideal anode materials for lithium rechargeable batteries with improved cycling life and high power capabilities [7-9]. In addition, oxidation of Sn nanowires has provided an alternative method to prepare sensitive SnO_2 nanowires for gas sensors [10]. Such exciting applications and the reliability evaluation (e.g., thermal instability [11]) have promoted the development of various strategies to grow Sn nanowires.

Several template-assisted synthesis methods have been attempted, in which Sn nanowires have been grown inside the nanochannels of anodized aluminum oxide or track etched polycarbonate membrane by electrodeposition using an aqueous solution containing Sn^{2+} ions [1, 2], and by solidification of the molten Sn injected with gas pressure [12] or hydraulic pressure [13]. Although the above template-assisted methods have offered the advantages of predefined morphology and size controllability, there still exist extrinsic shortcomings such as the troublesome template removal and possible chemical contamination [14]. Besides, successful growth of Sn nanowires following vapor-solid mechanism has also been reported by employing a noncatalytic and template-free vapor transport process [3]. In this case, the source of Sn vapor is required, which is obtained by ultra-high temperature (i.e., 973K) heating of Sn. Additionally, Xiao *et al*. [15] have grown Sn nanowires using thermal-stress-induced method by annealing a Si-Sn nanocomposite film in vacuum.

In this study, the same mechanism (i.e., thermal-stress-induced method) is employed to challenge the growth of Sn nanowires by using a multilayer thin film structure following thermal annealing in ambient environment. The effects of two vital influencing factors including surface morphology of

Sn film and annealing conditions are explored systematically.

2. Fundamentals and Experiments

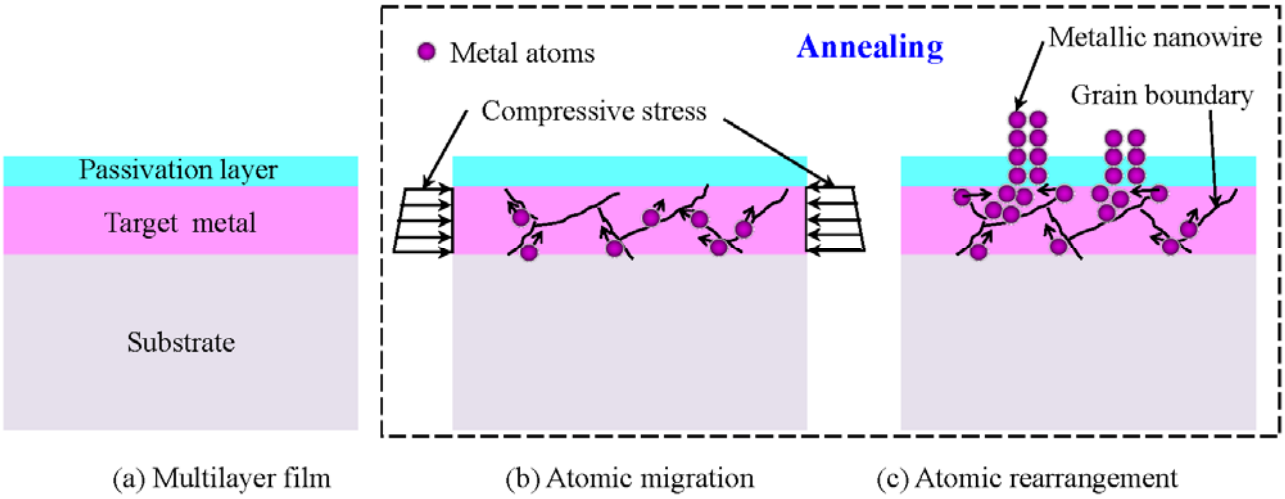

Fig. 1 Schematic thermal-stress-induced growth of metallic nanowires from a multilayer film

The mechanism of the present thermal-stress-induced growth of metallic nanowire using a multilayer is schematically illustrated in Fig. 1. A multilayer film shown in Fig. 1(a) is composed of three layers from top to down: passivation layer (e.g., natural oxide layer of Sn), target metal (e.g., Sn) and substrate (e.g., thermal oxidized Si). Because of the significant mismatch in the coefficient of thermal expansion (CTE) between target metal and substrate (α_{Sn} = 23.5×10^{-6}/K; α_{Si} = 7.6×10^{-6}/K [16]), the compressive thermal stress will be induced in target metal film during thermal annealing. Taking into account of material and geometrical singularities of the target metal film, the resulted local compressive stress gradient drives atoms migrating from more compressive areas to less compressive ones in the form of grain boundary diffusion and surface diffusion as shown in Fig. 1(b). With the accumulation of migrated atoms, the compressive stress gradient is generated between the interface of target metal/passivation layer and the free surface of passivation layer. Once the pressure resulted by the accumulated atoms attains a critical value, weak spots in the passivation layer will be broken and metallic nanowire will be formed through the rearrangement of metallic atoms. Based on the above growth mechanism, the similar multilayer thin film structure has been employed to fabricate various metallic nanowires, such as Cu [17], Bi [18], Ag [19], Al [20].

In the present work, a multilayer thin film structure for grow Sn nanowires are prepared. The Sn thin films are deposited on a 280μm-thick thermally oxidized Si wafer by radio frequency (RF) sputtering with an Ar flow of 20sccm and pressure of 5mTorr. The substrate temperature during sputtering is controlled to be room temperature (R.T.) by water cooling to assure thermal stress as high as possible in the following thermal annealing. By varying the RF power and sputtering time, a series of multilayer thin film structures are prepared in which the sputtered Sn films have different surface morphologies.

By using the obtained multilayer thin films, thermal annealing experiments are carried out at 473~503K for 2h in ambient environment. By observing the surface morphologies of the as-sputtered Sn films and the annealed ones using a scanning electron microscope (SEM), the effects of two vital influencing factors, including surface morphology of the as-sputtered Sn film and annealing conditions, are investigated.

3. Results and Discussion

3.1 Surface Morphologies of As-sputtered Sn Films

As a representative, the cross-sectional image of the prepared multilayer thin film is observed in Fig. 2 by using transmission electron microscope (TEM), in which the Sn film is sputtered at 20W and 240s. According to SEM observations, the surface morphologies of as-sputtered Sn films can be categorized into three representative sets, which are related to different RF power P and sputtering time t. For the films shown in Fig. 3 which are sputtered at RF power of 50W with sputtering rate of 1.5nm/s from 30s to 60s, the isolated island structure is clearly observed in each case. Moreover, the

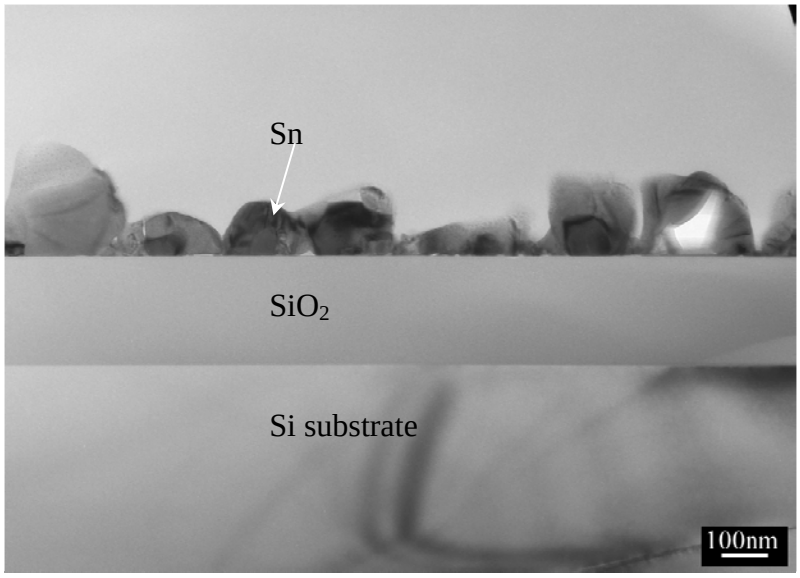

Fig. 2 Cross-sectional TEM image of the multilayer thin film (P=20W, t=240s)

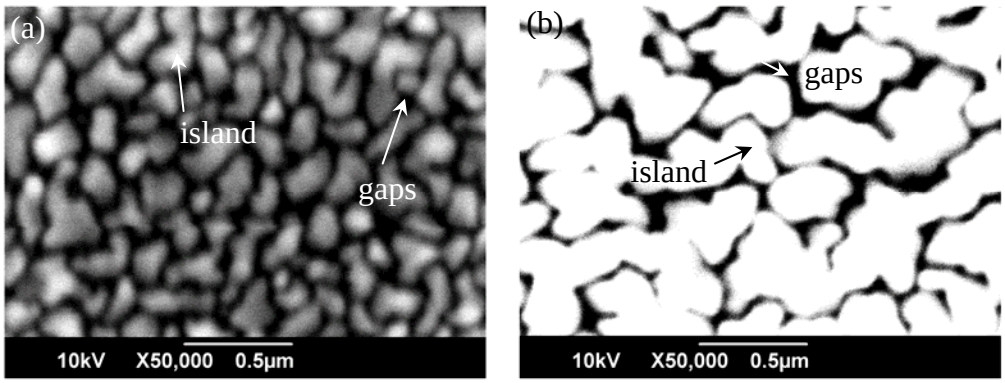

Fig. 3 Surface morphologies of Sn films with isolated island structure
(a) P=50W, t=30s; (b) P=50W, t=60s

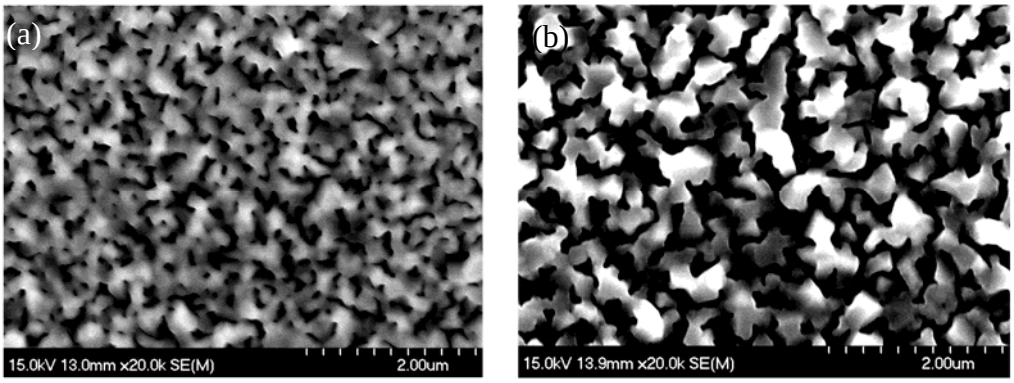

Fig. 4 Surface morphologies of Sn films with coalescent island structure
(a) P=50W, t=90s; (b) P=20W, t=240s

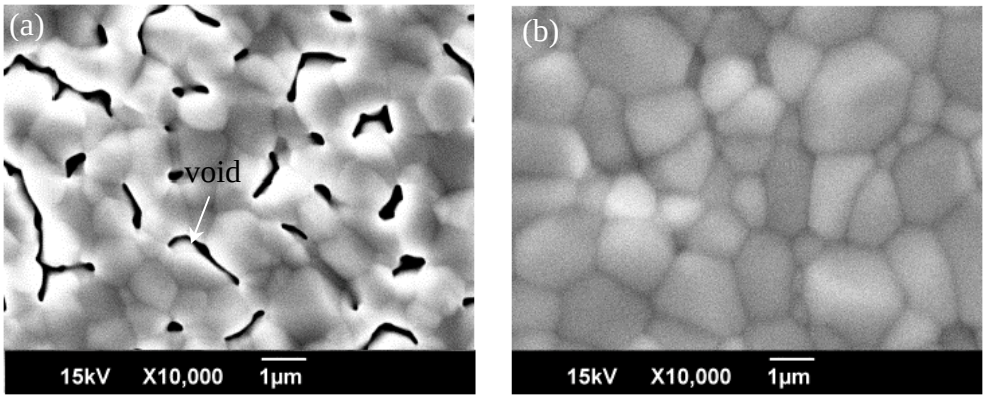

Fig. 5 Surface morphologies of Sn films with clear grains
(a) P=300W, t=125s; (b) P=300W, t=500s

size of island increases as the sputtering time increases. However, when the sputtering time increases to 90s, the isolated islands begin to coalesce with each other as shown in Fig.4 (a). This structure with coalescent islands is very similar with that in Fig. 4(b) sputtered at RF power of 20W for 240s with sputtering rate of 0.5nm/s. For films in Fig. 5 which are sputtered at RF power of 300W for 125~500s with sputtering ratio of 4nm/s, grain boundaries can be clearly observed. Interestingly, by comparing Fig. 5(a) and Fig. 5(b), it is found that with the sputtering time increases and the corresponding increasing film thickness, the voids at the grain boundaries decrease and finally vanish.

3.2 Surface Morphologies of Annealed Sn Films

The surface morphologies of the above as-sputtered Sn films after annealing at 473~503K for 2h are given in Fig. 6. Significant changes on the surface morphologies are only observed for Sn films which are sputtered under the following three conditions: (I) P=50W, t=90s (Fig. 6(a)); (II) P=20W, t=240s (Figs. 6(b, d)); (III) P=300W, t=500s (Fig. 6(c)). At the annealing temperature of T=473K, large numbers of hillocks shown are observed on the films sputtered at the above three cases (i.e., Figs. 6(a~c)) while no any change is found on the other films. When the annealing temperature is increased up to T=503K, large numbers of whiskers with various shapes are only observed on the film sputtered at P=20W (Fig. 6(d)). The representative images of hillock or whisker are shown in in Fig. 7. These distinctive differences can be discussed as below: for the sputtered Sn films with

isolated islands or voids in grain boundaries, it is difficult to result in stress concentration because of the existence of gap or voids. On the other hand, for Sn films with dense grains or coalescent islands, it is possible to induce thermal stress during the annealing with consideration of material and geometrical singularity. It should be noted that for the former (i.e., Sn film with dense grains) with thickness in micro-scale, the part of internal stress is released by recrystallization during the formation of grains. However, for the latter (i.e., Sn film with coalescent islands) with thickness in nanoscale, the induced thermal stress is much higher than that in the former.

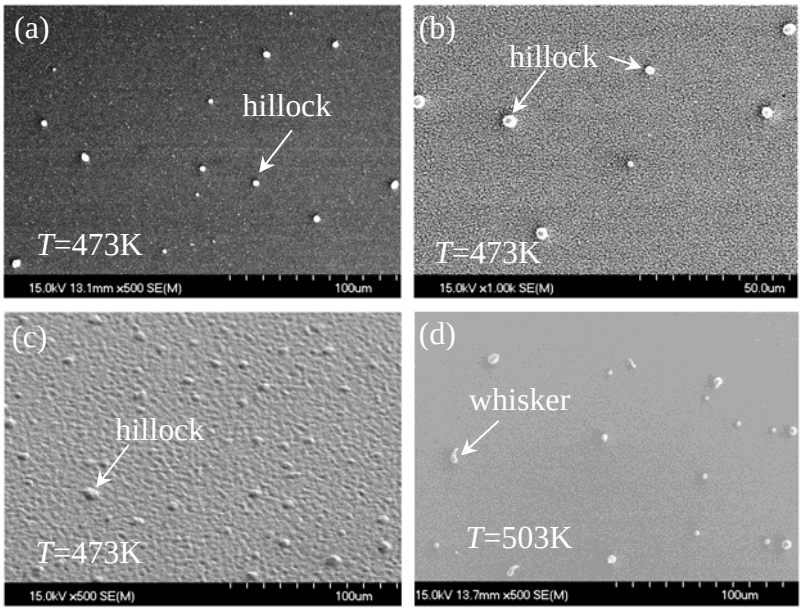

Fig. 6 Surface morphologies of annealed Sn films
(a) P=50W, t=90s; (b,d) P=20W, t=240s; (c) P=300W, t=500s

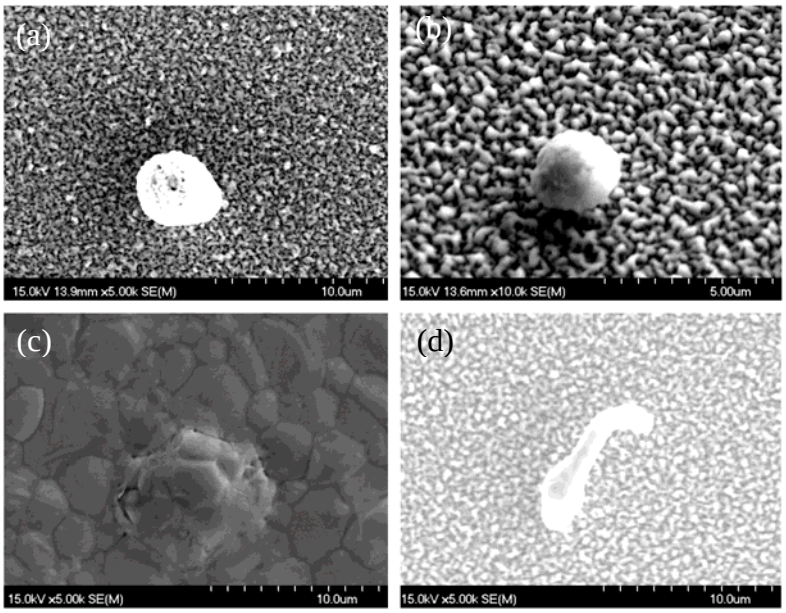

Fig. 7 Representative hillock or whisker in annealed Sn films
(a) P=50W, t=90s; (b,d) P=20W, t=240s; (c) P=300W, t=500s

4. Conclusions

By employing a multilayer thin film structure composed of thermally oxidized Si substrate and sputtered Sn film, a series of thermal annealing experiments are carried out to challenge the growth of Sn nanowires using thermal-stress-induced method. The effects of two vital influencing factors, i.e., surface morphology of Sn film and annealing conditions, are explored systematically. For Sn films with either isolated island structure or voids in grain boundaries, there is no any change on surface morphology after annealing. Such behavior can be attributed to the existence of gaps among islands or voids in grain boundaries, which make it difficult to generate sufficient stress to make Sn nanowires grow. On the other hand, for Sn films with dense grains or coalescent islands, the occurrence of hillocks or whiskers after annealing indicates that the proper control of surface morphology of Sn film and annealing conditions may grow Sn nanowires with large aspect ratio.

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