EXPLICIT EXPRESSION FOR STRESS IN MULTI-LEVEL LINE STRUCTURES AND IN CONNECTING VERTICAL VIAS

Ares J. Rosakis[1], Tae-Soon Park[1], and Subra Suresh[2]
[1] Graduate Aeronautical Laboratories, California Institute of Technology, Pasadena, CA 91125
[2] Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139

ABSTRACT

Explicit expressions for volume-averaged thermal stresses in periodic metal and dielectric lines at a single Damascene layer deposited on a substrate are first presented. Individual stress components acting on these structures are expressed in terms of substrate curvature, temperature change, elastic properties and thermal expansion coefficients of individual phase. By observing that such stresses at different metalization levels are not influenced by the presence of additional layers, these expressions for the stress components in terms of total substrate curvatures are subsequently generalized to multi-level line structures by recourse to the concept of superimposition. For via plugs connecting lines at different metalization levels, the vertical stress component is also calculated in terms of the vertical stress components at the top and bottom lines and of mismatch stress from embedding dielectric materials. This stress component is directly related to critical tensile (via pull-out) and compressive (via push-in) failures of the via plugs recently reported in the literature. Full three-dimensional finite element analysis (FEA) is carried out for the purpose of verifying the generalized analytical stress models for both line and via structures. The analytically predicted and numerically calculated stress components are found to compare very well. Finally, thermal compatibility of various low-k dielectric materials with Cu is discussed in relation to probable failure mechanisms associated with the predicted stress amplification phenomenon at the vertical via plugs.

Keywords: Cu lines, low k dielectrics, multi-level metalization, stress-induced failure, thermal stress, vertical via structures

1 INTRODUCTION

The ongoing trend within the semiconductor industry towards larger wafers with ever smaller circuit features (e.g. metal lines and vertical via plugs connecting up to 9 levels of metalization) necessitates the implementation of advanced modeling tools that are able to predict the propensity of failures in micro- and nano-features. It also necessitates the development of inspection and measurement methodologies that are capable of gathering data rapidly over a large area and in a variety of manufacturing environments. Since 2001, the industry has been scaling up from 200mm to 300mm diameter wafers which host hundreds of repeated structures (dies) with millions of circuit features whose minimum dimensions are currently of the order of 100nm. The industry projects reduction of critical feature dimension to 65nm by late 2005 and to 45nm by early 2007 to be followed by the gradual introduction of 450mm wafers by early 2008 [1]. While the progressively phased out 200mm wafers feature yield levels of over 95%, the new generation of 300mm wafers are currently limited to 65% yield levels. Only half of this yield loss is properly accounted for. However, there are several critical issues that are well known to compromise yield as the trend for larger wafers and smaller features continues. Such problems are related to the fact that (1) wafer flatness, (2) thin film or micro-feature uniformity and (3) thermal and residual stress built up, resulting from multiple film deposition, anneal, and curing steps are inherently more difficult to control in such large, thin structures.

Classical plate bending theories provide a fundamental link between the curvature of a substrate and the thickness-averaged stresses developed in the thin films and micro- and/or nano-features deposited on it [2-6]. Accumulated stress-induced damage and failure in such ever-diminishing circuit features that are deposited on ever larger, thinner and flimsier substrates

(susceptible to larger curvatures) become more prevalent and manufacturing yields decrease accordingly. The stresses may lead to device failure in Cu by a variety of phenomena such as stress-induced nucleation of voids [7] (e.g. during the cooling phase following passivation, creep-induced void growth during thermal cycling), electromigration [8, 9], and hillock formation [10] during a period of service. As new, low strength, low-k dielectric materials (e.g. Black Diamond, SILK or the newly introduced class of porous organosilicates) are being evaluated to replace silicon oxide, the embedding of metal lines, introduces a host of new stress-induced failure mechanisms. These include interface delamination, and barrier layer and dielectric cracking [11, 12], which are known to be major contributions to yield loss. The rate of yield loss is getting higher as the industry is pushing for ever increasing levels of metalization (high need of more integrated semiconductor chips) deposited on wafers of ever increasing diameters (smaller thickness to diameter aspect ratios). Among failure mechanisms associated with multi-level interconnect structures, pull-out or push-in of the via plugs connecting lines at different metalization levels is reported to occur during thermal cycling and/or after annealing. The nature of such mechanisms depends on the selection of embedding dielectric materials [13, 14]. Indeed voiding in vertical vias remains a problem even in cases where voiding in lines has successfully been suppressed suggesting the occurrence of a mechanism of stress amplification in the vertical via plugs.

In this work, explicit expressions for volume-averaged thermal stresses in the metal and dielectric lines at a single periodic Damascene layer on a substrate are first presented. Based on the above stated conclusions, from our previous research, which shows that stresses in lines at different metalization levels are not much influenced by the presence of additional layers, the explicit expressions for the stress components in terms of, temperature-induced, substrate curvature changes are generalized to multi-level line structure by recourse to the concept of superimposition. For via plugs connecting lines at different metalization levels, the vertical stress component is also calculated in terms of the vertical stress components at the top and bottom lines and of the mismatch stress resulting from the interaction of the via metal with the embedding dielectric materials. Vertical stresses in the connecting vias are found to be amplified in relation to their counterparts in the top and the bottom line layers. This stress component is directly related to critical tensile (via pull-out) and compressive (via push-in) failures of the via plugs recently reported in the literature [13, 14]. Full three-dimensional finite element analysis (FEA) is carried out for the purpose of verifying the generalized analytical stress models for both line and via structures. The analytically predicted and numerically calculated stress components are found to compare very well. Finally, thermal compatibility of various dielectric materials with Cu is discussed in relation to probable failure mechanisms associated with the predicted stress amplification phenomenon at the vertical via plugs.

2 ANALYTICAL AND NUMERICAL MODELING

2.1 ANALYTICAL MODELING

Figure 1 is a schematic of metal interconnect lines (e.g. copper) with dielectric lines (e.g. oxide) placed on a Si substrate following the Damascene process, Cu CMP and subsequent capping layer deposition. In Fig. 1, t, b, d and h_f represent the height and the width of the lines within the periodic structure, the spacing between lines and the net height of a periodic unit, respectively. The height of the capping layer is equal to (h_f-t). Consider now a scenario in which such a structure, composed of tall lines (t/b>>1) and featuring no capping layer (h_f=t), experiences a change of temperature, ΔT, from a reference state (e.g. an initial stress-free state such as cooling from annealing or from passivation). As a result of this temperature change, the entire composite, metal line/dielectric film structure will develop two non-zero (in-plane) volume-averaged stress components, $<\sigma_{xx}>$ and $<\sigma_{yy}>$, due to the mismatch of thermal expansion coefficients between the

substrate and the homogenized composite thin film structure. These stress components represent averages over the entire composite film structure of height, *t*. In addition, both metal and dielectric lines will also develop stresses whose three non-zero volume-averaged (over the metal or dielectric line cross-sections) components will be denoted by $<\sigma_{xx}^{l}>$, $<\sigma_{yy}^{l}>$ and $<\sigma_{zz}^{l}>$ and $<\sigma_{xx}^{o}>$, $<\sigma_{yy}^{o}>$ and $<\sigma_{zz}^{o}>$, respectively. Such a scenario, featuring a single level Damascene structure of tall lines without a capping layer, was considered in our previous analysis [5] in which an implicit relation between the temperature change and the stress was developed. By analytically inverting this relation, one can express the stresses on the metal lines (superscript *l*) explicitly in terms of the volume-averaged stresses acting over the entire composite film structure and temperature change as follow:

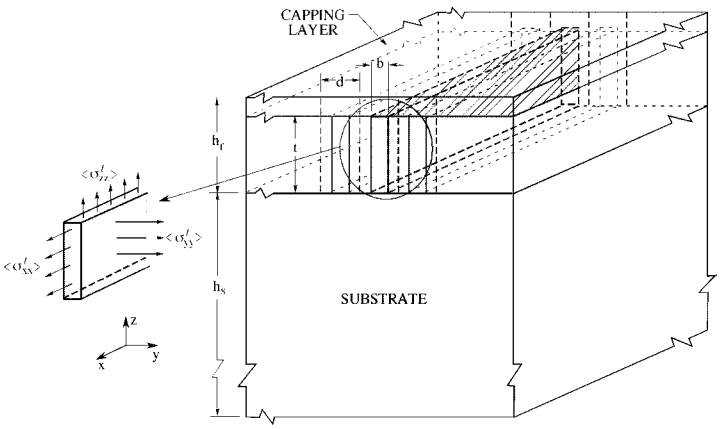

Figure 1. Schematic of a single level, periodic Cu interconnect line structure with a capping layer on a Si substrate. High line aspect ratio case (tall lines).

$$\left\langle \sigma_{ij}^{L} \right\rangle = \left\langle \sigma_{ij}^{L} \right\rangle (b/d,\ \mathrm{E_L},\ \mathrm{E_o},\ \mathrm{E_s},\ \nu_{\mathrm{L}},\ \nu_{\mathrm{o}},\ \nu_{\mathrm{s}},\ \alpha_{\mathrm{L}},\ \alpha_{\mathrm{o}},\ \mathrm{t},\ \mathrm{h_s},\ \Delta\kappa_{\mathrm{x}},\ \Delta\kappa_{\mathrm{y}},\ \Delta T) \qquad (1)$$

Figure 2 shows a representative structure composed of vertical vias connecting horizontal periodic lines at the lower and upper levels following a Dual Damascene process and capping inter-layer deposition. The vias are cylindrical and periodic with a diameter of 2*R*, a pitch of *V*, and a height of $h_v=h_f-t$. As in Figs. 1 and 2, the vias connect horizontal lines of width *b* and pitch *d*. The material between the top of the lower line features and the bottom of the upper line features, surrounding the vias, is filled with the capping inter-layer dielectric (ILD) described in the previous section (materials properties E_c, ν_c, α_c). The

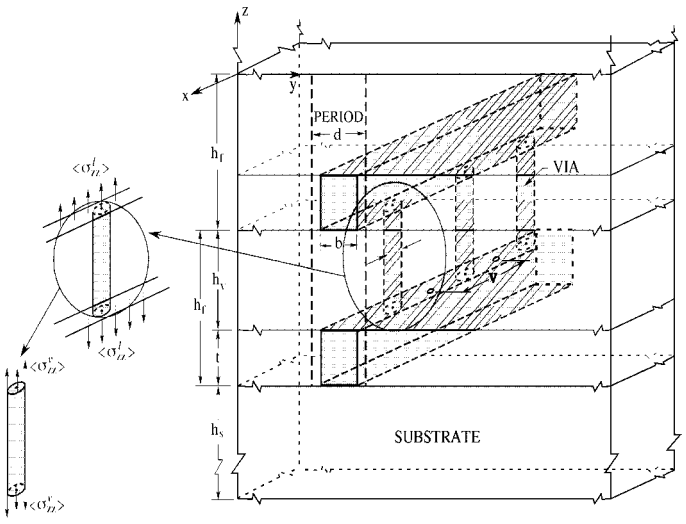

Figure 2. Schematic of a two level, periodic Cu interconnect line structure with vertical connecting vias at the lower and at the upper levels. Stress transfer at the vias is illustrated.

average vertical stress in each via is now given as follow:

$$\left\langle \sigma_{zz}^{v} \right\rangle = \left\langle \sigma_{zz}^{v} \right\rangle (f_v, E_v, E_c, \alpha_v, \alpha_c, \left\langle \sigma_{zz}^{L} \right\rangle, \Delta T) \quad (2)$$

Figure 3 shows computed amplification factors (ratios of $<\sigma_{zz}^{V}>$ /$<\sigma_{zz}^{l}>$) as a function of the volume fraction of vias f_v for two commonly used encapsulating or passivating dielectrics (e.g. commercial materials under the trade names of TEOS and SILK) of a structure whose adjacent periodic line structures are connected by either Cu or W vias and is subjected to a ΔT=-380°C. The purpose of the figure is to use different material combinations to investigate the effect of material (mechanical and thermal) properties mismatch on the establishment of stress concentration in vias. When a stiff metal (e.g. W) is used for a via plug, the vertical stresses are amplified to a much higher level in the vias (compared to their line equivalents), especially when the via volume fraction is small. When the embedding dielectric is compliant (e.g. polymer-based dielectric materials such as SILK), the vertical stress in the via become very high for isolated vias.

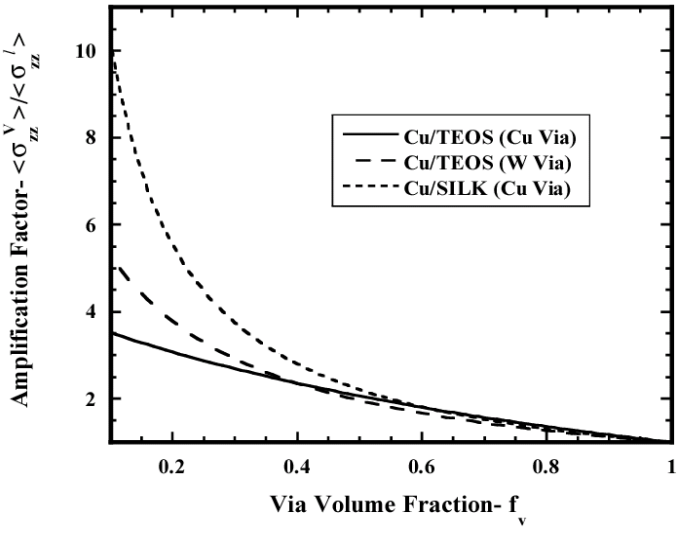

Figure 3. Ratios of volume-averaged stresses of connecting vertical vias to corresponding stress values of adjacent lower and upper lines as a function of via volume fractions based on analytical predictions.

2.2 NUMERICAL MODELING

A full three-dimensional finite element method (FEM) was used to verify the present analytical model. For this purpose, the finite element program ABAQUS [15] was employed. Table 1 shows the material properties used in the simulations. In this work, Cu was chosen as the material for the periodic metal lines and vertical vias in light of the shift from conventional Al-based interconnects to new Cu Damascene structures in the semiconductor industry. For embedding dielectrics, not only conventional materials (e. g. SiO_2), but also newly emerging low-k dielectric materials were employed in the numerical simulations in order to investigate their mechanical compatibility with the Cu interconnect lines/vias. The materials were assumed to be linear thermo-elastic and isotropic while residual stresses, which may have resulted from Cu deposition and/or polishing, were not considered in the calculation. Indeed, the goal of this analysis is to calculate the stress changes in the line features resulting from changes in temperature ΔT. However, the thermo-elastic constitutive law used here is expected to be valid over a wide temperature range of practical interest since the material surrounding the Cu lines and vias leads to elevated levels of hydrostatic stress. This stress induces highly constrained deformation within the Cu and retards plastic deformation [16].

A representative unit cell (top portion) and the finite element discretization used in the 3-D numerical simulation are shown in Fig. 4. For the purpose of visualization, the elements

representing the inter-layer dielectric (ILD) are not shown. Vias with circular cross-sections are considered in this simulation. For this calculation, the periodicity and symmetry facilitate the use of only a single unit segment which ranges from the two symmetry planes to the neighboring periodic boundaries (see Fig. 4). Details of the periodic boundary conditions are described in our previous work [5].

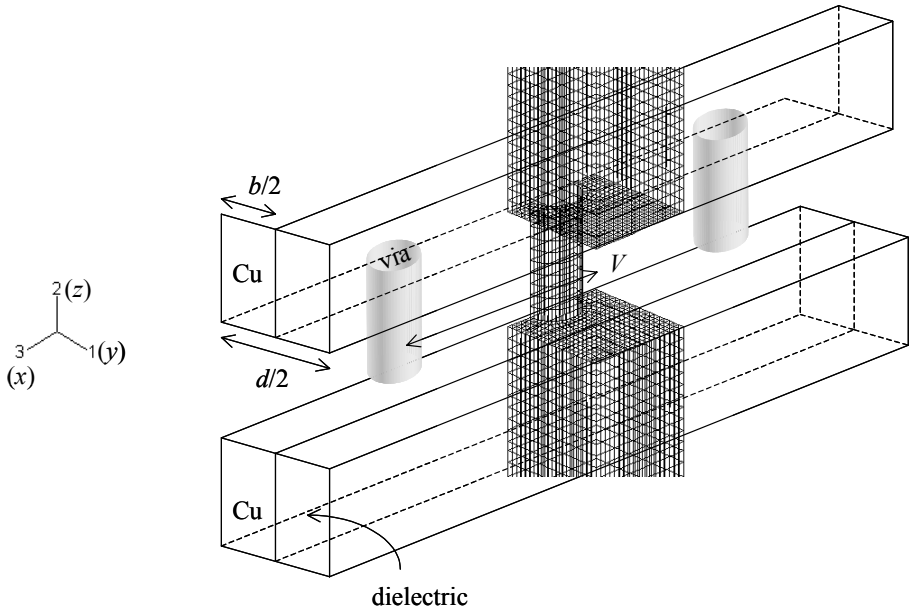

Figure 4. A representative unit cell (top portion) and finite element discretization used in the 3-D numerical simulation (elements of the inter-layer dielectric (ILD) not shown).

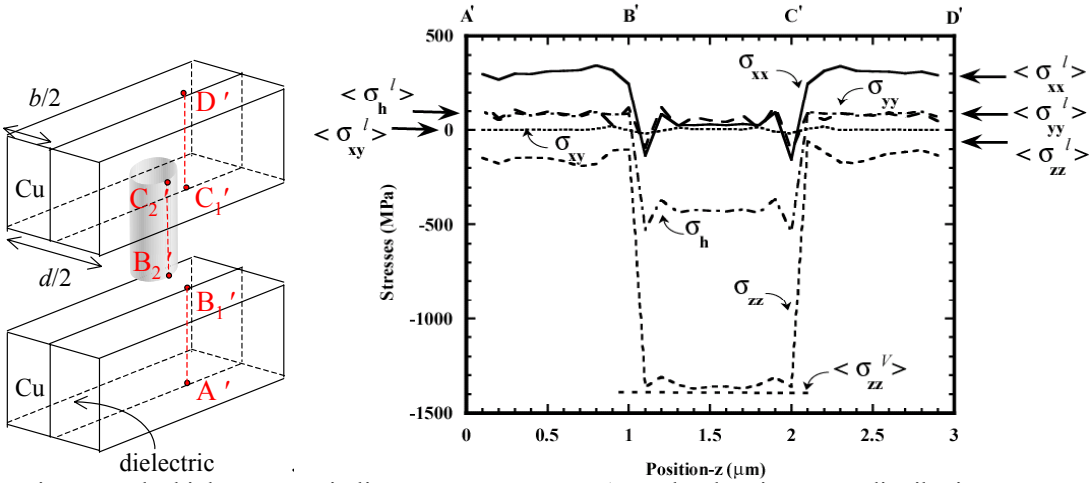

Figure 5. The high aspect ratio line geometry case. FEA results showing stress distribution along the path in the schematic (along the vertical interfaces between lines/via and an embedding dielectric) from the bottom of the lower line through the via to the top of the upper line. Analytical predictions are also indicated for each feature.

Figure 5 shows FEA results on stress variations in elements lying along the path of the schematic (path along the interfaces between lines/via and an embedding dielectric) ranging from the bottom of the lower line, through the via, to the top of upper line. Stress values are fairly constant within each region. All stress components (both normal and shear stresses) are extremely well matched with analytical predictions on upper/lower lines and a via.

3 CONCLUSIONS

For vertical via plugs connecting lines at different metalization levels, explicit expression for the volume-averaged vertical via stress component is also presented in terms of the volume-averaged vertical stress components at the upper and at the lower lines and of the mismatch stresses between the vias and the embedding inter-layer dielectric materials. It is found that the vertical via stresses are ``amplified'' in relation to the vertical stresses in the upper and lower lines. This stress amplification is a function of dielectric material choice, of line and via geometry. The accuracy of the generalized analytical stress models for both line and via structures are verified by using full three-dimensional finite element analysis (FEA). The analytically predicted and numerically calculated stress components are found to compare very well for a variety of material properties and line/via geometries. This is particularly true for line/via geometries featuring lines of high aspect ratio, consistent with the assumptions of the theory (see Fig. 5).

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